

Multiscale Modeling of Nanowire-based Schottky-Barrier Field-Effect Transistors for Sensor Applications

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We present a theoretical framework for the calculation of charge transport through nanowire-based Schottky-barrier field-effect transistors that is conceptually simple but still captures the relevant physical mechanisms of the transport process. Our approach combines two approaches on different length scales: (1) the finite elements method is used to model realistic device geometries and to calculate the electrostatic potential across the Schottky-barrier by solving the Poisson equation, and (2) the Landauer approach combined with the method of non-equilibrium Green's functions is employed to calculate the charge transport through the device. Our model correctly reproduces typical I-V characteristics of field-effect transistors and the dependence of the saturated drain current on the gate field and the device geometry are in good agreement with experiments. Our approach is suitable for one-dimensional Schottky-barrier field-effect transistors of arbitrary device geometry and it is intended to be a simulation platform for the development of nanowire-based sensors.

I. INTRODUCTION

Over the last few decades one-dimensional (1D) semiconducting silicon-nanowires (SiNWs) have been widely studied as potential building blocks for future electronic devices due to their excellent electrical performance, small size, and controllable bottom-up fabrication.¹⁻⁴ Many types of SiNW devices such as ultrasensitive sensors,^{5,6} photodetectors,⁷ and bipolar field effect transistors (FETs)^{8,9} have been reported. The key issue for sensor applications is the down-scaling of FETs to one dimensional structures, such as nanowires. The attractive feature of nanowire-based FETs is that the binding of charged species can be directly monitored by the change in current through the NWs because of their high surface-to-volume ratios and small cross-sectional conduction pathways.

Recently Weber *et al.* have reported dopant-free Schottky-barrier (SB) FETs consisting of intrinsic SiNWs working as a channel and NiSi₂ nanowires working as source and drain contacts with gate lengths down to subphotolithographic values.¹⁰⁻¹³ Their devices are based on single-crystalline SiNWs into which nickel atoms are diffusing from both ends of the wire, forming sharp interfaces between NiSi₂ “leads” and a Si “channel” in the center. The channel length depends on the annealing time. Measurements of their transport characteristics have shown the highest on-current and on-conductance values recorded to date for intrinsic SiNW-FETs. It is advantageous that the silicon channel is dopant free since the noise caused by structural impurities is greatly reduced compared to doped nanowires. This feature is beneficial for the production of reliable SiNW-based biosensors.

By modifying the surface of the SiNWs with DNA,^{6,14-17} enzymes¹⁸ or other chemical compounds⁵

many kinds of biosensors such as EnFET (enzyme FETs), Immuno-FETs,¹⁹ and DNA-FETs have been demonstrated. Thus, SiNW-based SB-FETs are expected to provide a promising platform for biosensor applications.

For a better understanding of the basic charge transport characteristics through the SiNW-based SB-FETs and the development of the NW-based biosensors, it is essential to systematically reveal the factors controlling the charge transport through a pristine FET device.

Several approaches to describe the electronic transport through 1D SB-FETs have been proposed. Knoch *et al.* developed quantum mechanical simulations of a ultrashort channel n-metal-oxide-semiconductor FETs (n-MOSFETs) on silicon on insulator (SOI)²⁰ and of a SB-FETs on SOI²¹ using real-space non-equilibrium Green's function formalism. Heinze *et al.* introduced a method to calculate the transport through carbon nanotube (CNT) SB-FETs using the Landauer formula and the WKB approximation.²² Pourfath *et al.* extended this approach to cylindrical double-gate CNT SB-FETs.²³ Michetti *et al.* expressed the conduction band by an analytical formula and calculated the transmission functions analytically.²⁴ Appenzeller *et al.* have investigated the transport properties of CNT-FETs and SiNW-FETs in detail.²⁵ They used a modified 1D Poisson equation and the non-equilibrium Green's function technique to calculate the transmission function with the finite difference method in 1D. Jimenez *et al.* expressed the conduction band profile by an analytical expression^{26,27} and calculated the transport properties of SB-FETs by using the WKB approximation, corrected with k-matching conditions for MSi₂/Si(111) and MSi₂/Si(100) (with M=Ni, Co, and Fe) interfaces.²⁷

The majority of these approaches were applied to highly symmetric devices such as cylindrical FETs designed for integrated circuits. In these systems, the sym-

metry significantly reduces the computation time. However, to simulate realistic devices for sensor applications, a computationally cheap model that is applicable to arbitrary device geometries is also desired. The multiscale model presented in this article was developed for this purpose. Our method combines two approaches on different length scales: (1) the finite elements method (FEM) is used to calculate the three-dimensional (3D) electrostatic potential across the Schottky-barrier by solving the Poisson equation for realistic device geometries. Then we extract the 1D potential profile along the axis of the NWs and use (2) the Landauer approach combined with the method of non-equilibrium Green's functions^{28–30} to calculate the charge transport through the device. Our model is conceptually simple, computationally inexpensive, it uses only a few empirical parameters, and it is easily expandable. Since the method is non-atomistic the number of atoms in the system is irrelevant and therefore it is possible to simulate devices with dimensions ranging from a few nanometers up to some micrometers.

In this work we model pristine SB-FETs consisting of SiNWs and NiSi₂ NWs. We analyze the influence of the device geometries such as gate lengths, thickness of the insulators, and the gate voltages on the charge transport through the SB-FETs. Despite the simplicity of the model, the numerical calculations show I-V characteristics of typical conventional MOSFETs and the calculated saturation currents are in good agreement with the experimental results by Weber *et al.*¹⁰

This paper is organized as follows. Section II presents theoretical framework of multiscale modeling and section III shows the computational details and parameter settings. In section IV, we present dependence of the electrostatic potential on device geometries, investigate transmission profiles and I-V characteristics of test systems, and compare the numerical results with the reported experimental results. Finally, we summarize this paper in section V, emphasizing the simplicity and versatility of the multiscale modeling.

II. THEORETICAL FRAMEWORK

Figure 1 shows a schematic image of a SiNW-based SB-FET. The device consists of a SiNW working as a channel and NiSi₂ segments working as source and drain contacts. This nanowire is put on the gate contact covered with SiO₂. The source, drain, and gate voltages, V_S , V_D , V_G , the NW diameter d_{NW} , as well as the length of the silicon nanowire channel L_C , and the thickness of the oxide layer t_{ox} are all indicated in figure 1.

The band diagram of the electronic transport process through a SB-FET under an applied source-drain voltage with different gate voltages is shown in figure 2. The energy gap Φ_{SB} between the edges of the conduction band (CB) of the silicon channel and the Fermi energies of the NiSi₂ contacts is called the Schottky-barrier. The barrier thickness is reduced with increasing gate voltage,

allowing the electron in the source to tunnel through the potential energy barriers.^{22,25,31} Thus, the drain current at the constant source-drain voltage is controlled by the gate voltage. The charge transport through the SB-FET can be divided into three stages (see figure 2): 1. electron (hole) injection into the conduction band (valence band) by tunneling through the Schottky-barrier in the left interface; 2. ballistic or diffusive transport of charges through the SiNW; 3. tunneling of charges through the Schottky-barrier in the right interface.

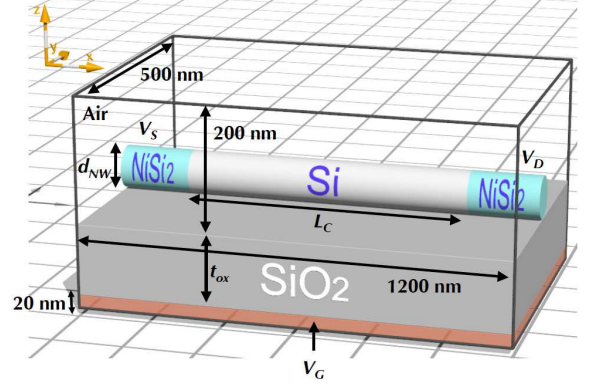


FIG. 1: A model of a SiNW-based Schottky-barrier FET with realistic dimensions, as considered in this work. V_S , V_D , V_G are source, drain, and gate voltages, respectively. L_C is the length of the silicon nanowire channel, and t_{ox} is the thickness of the oxide layer. d_{NW} is the diameter of the silicon nanowire.

According to figure 2 we define the 1D potential energy profile $U(x)$ along the axis of the NiSi₂/Si/NiSi₂ nanowire as

$$U(x) = \begin{cases} \mu_L - \Phi_L & (x < 0) \\ \mu_L + \Phi_{SB} + U_{ES} & (0 \leq x \leq L_C) \\ \mu_L - eV_{SD} - \Phi_R & (L_C < x) \end{cases}$$

where the position $x = 0$ is set to be at the left NiSi₂/Si interface, $\mu_{L/R}$ is the chemical potential of the left/right contact, Φ_{SB} is the Schottky-barrier energy, $\Phi_{L/R}$ is the ground potential for left/right contact, V_{SD} is the applied source-drain voltage, and $U_{ES}(x)$ is the 1D electrostatic potential along the axis of the Si-NW obtained from FEM calculations (see below). For the Schottky-barrier energy Φ_{SB} we use experimental values from the literature (see below). The ground potential $\Phi_{L/R}$ is introduced in order to define the baseline for the transmission calculation at the two interfaces. The two ground potentials are chosen to span the bias window, i.e., $\Phi_L = eV_{SD}^{max}$, where V_{SD}^{max} is the maximum source-drain (bias) voltage that is used in a set of calculations, and $\Phi_R = 0$. This is how the energy of the electrons in the source that are within bias window is set higher than the ground potential. In order to calculate the charge transmission at the two interfaces (see bottom of figure 2) we use

$U(x)$ in the interval $x = [-1.5\text{nm} \dots 21.5\text{nm}]$ for the left and $x = [L_c - 21.5\text{nm} \dots L_c + 1.5\text{nm}]$ for the right interface. In these two ranges the potential inside the SiNW ($0 \leq x \leq L_c$) is regularized by applying an energy cutoff U^{cut} such that $U(x) = U^{\text{cut}}$ for energies smaller than U^{cut} . At the left (L) and right (R) interfaces the cutoff energy is $U_{L/R}^{\text{cut}} = \mu_{L/R} - \Phi_{L/R}$, i.e., $U(x)$ is never smaller than the ground potential $\Phi_{L/R}$ (see also figure 5).

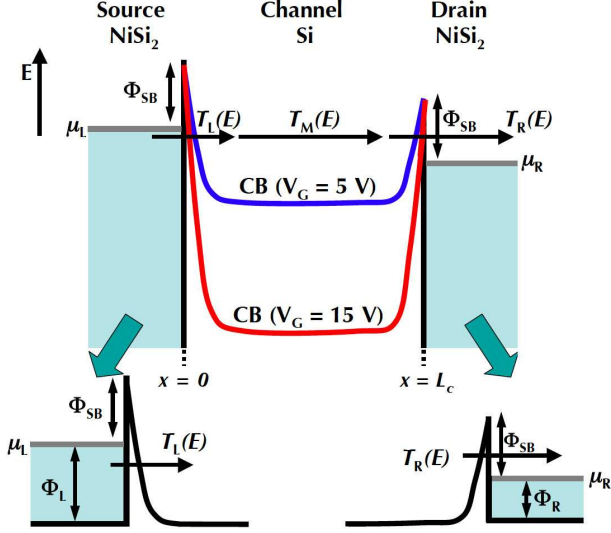


FIG. 2: An energy diagram of a SiNW-based Schottky-barrier FET under an applied source-drain voltage with different gate voltages V_G . The charge transport can be divided into 3 processes; coherent tunneling through the Schottky-barrier $T_{L/R}(E)$ at the left/right interfaces and ballistic transport $T_M(E)$ in the middle. Increasing the gate voltage leads to stronger bending of the conduction band (CB), which reduces the width of the Schottky-barrier. Φ_{SB} is the height of the Schottky-barrier. $\mu_{L/R}$ and $\Phi_{L/R}$ are the chemical potential and the ground potential for left/right contacts, respectively.

In this study, we employed the Landauer approach in *real-space* for the calculation of the electron transmission through the NiSi₂/Si interfaces.^{25,32–34} The Hamilton operator in 1D is given by

$$\hat{H} = -\frac{\hbar^2}{2m_{\text{eff}}} \frac{d^2}{dx^2} + U(x),$$

where m_{eff} , and $U(x)$ are the effective mass of electrons (or holes) and the potential energy profile along the axis of the nanowire, respectively. Using finite differences on an equally spaced grid, the Hamilton matrix is given by^{33–35}

$$H_{n,m} = (U_n + 2t_0)\delta_{n,m} - t_0\delta_{n,m+1} - t_0\delta_{n,m-1},$$

where $U_n = U(x_n)$ is the potential, $x_n = an$ is the position, a is the grid spacing, and $t_0 = \hbar^2/2m_{\text{eff}}a^2$.

The transmission functions at the left (L) and right (R) interfaces are obtained via the Landauer-Büttiker formalism using the Fisher-Lee relation:

$$T_{L/R}(E) = \text{Tr}[G^R \Gamma_{L/R} G^A \Gamma_M],$$

where Tr being the trace operation and Γ_α ($\alpha = L, R, M$) are the broadening functions for the contacts, given by $\Gamma_\alpha(E) = i[\Sigma_\alpha(E) - \Sigma_\alpha^\dagger(E)]$. Γ_M is the auxiliary broadening function, which is required because the system is cut into two 1D tunneling problems. The self-energies are defined as $\Sigma_\alpha(E) = -t_0 \exp(ika)$, where ka is obtained by inverting the band dispersion of the 1D wire (linear chain) $E(ka) = U_\alpha + 2t_0(1 - \cos(ka))$, and $U_\alpha = U(x_\alpha)$ ($\alpha = L, R, M$) is the potential at the position of the left/right/auxiliary contacts.^{33–35} Note that the Σ_α is a diagonal matrix and its matrix elements are zero except for the position where the left/right/auxiliary contact is attached.

The retarded/advanced Green's functions $G^{R/A}$ for the left (L) and right (R) interfaces are defined as

$$G^{R/A}(E) = [(E \pm i\eta)I - H - \Sigma_{L/R} - \Sigma_M]^{-1},$$

where $i\eta$ is an infinitesimal imaginary value, I is the identity matrix, $H = H_{n,m}$ is the Hamilton matrix, and Σ_α ($\alpha = L, R, M$) are the self-energy matrices as defined above.

Assuming ballistic charge transport through the silicon channel, i.e. $T_M(E) \simeq 1.0$, and ignoring the phase memory, the total transmission through the device is given by³³

$$T(E) = T_L T_R / (T_L + T_R - T_L T_R).$$

The assumption of ballistic transport in the core channel region was validated experimentally for devices having channel lengths less than $1 \mu\text{m}$.¹⁰

Finally, the current through the SB-FET is calculated from

$$I_{SD} = 2e/h \int_{-\infty}^{\infty} T(E)(F_L(E) - F_R(E)) dE.$$

The term $F_{L/R}$ is the effective Fermi function k -summed over the transverse modes in the $y-z$ plane, represented by

$$F_{L/R}(E) = S m_{\text{eff}} k_B T / \pi \hbar^2 \ln(1 + \exp((\mu_{L/R} - E)/k_B T)),$$

where S and $\mu_{L/R}$ are the cross-sectional area of SiNWs and the chemical potential for left/right electrodes, respectively. Under an applied source-drain voltage V_{SD} , the chemical potential for the right electrode is given by $\mu_R = \mu_L - eV_{SD}$.

Note that the same formalism works for hole currents by changing the band of interest from the conduction band (CB) to the valence band (VB), the Fermi function from $F_{L/R}(E)$ to $1 - F_{L/R}(E)$, effective mass of electron to effective mass of hole, and exchanging the sign of the gate voltages.²⁶

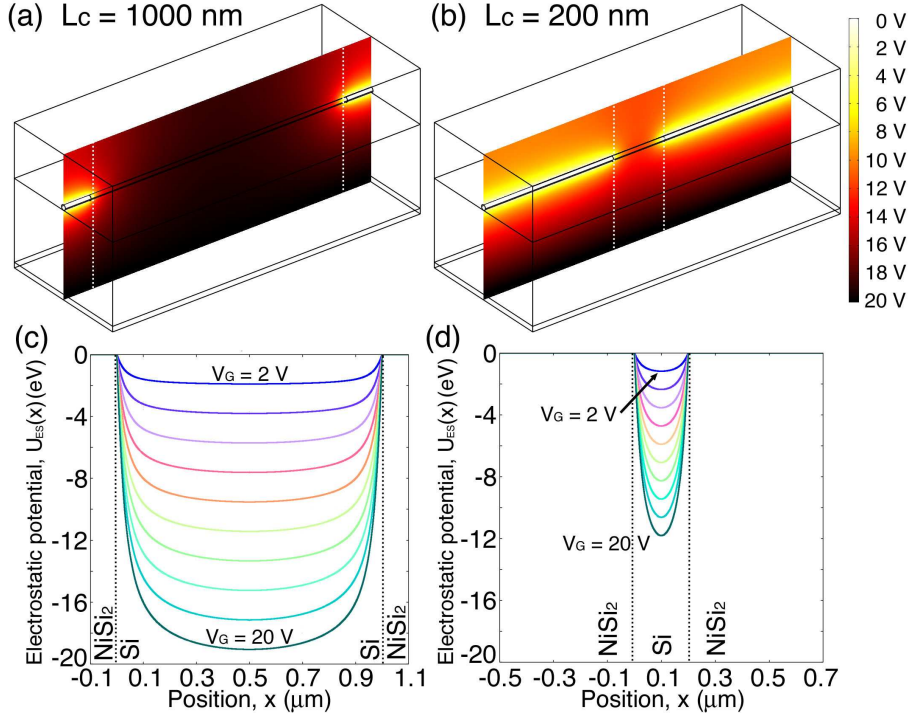


FIG. 3: Electrostatic potential U_{ES} of the SiNW-based Schottky-barrier FETs with different channel lengths being $L_c = 1000$ nm in (a)/(c) and $L_c = 200$ nm in (b)/(d). Top: $U_{ES}(x, z)$ in the $y = 0$ plane; bottom: $U_{ES}(x)$ along the axes of the corresponding wire. In these plots the metallic NiSi₂ nanowire is held at $U = 0$ V. The variation of the electrostatic potential is strongest close to the contacts.

III. COMPUTATIONAL DETAILS

In this work we assumed that the effective electron mass of whole system for holes/electrons is equal to that of free electron. For all calculations we use $\mu_L = 0$ eV, $a = 1.0$ Å, $m_{\text{eff}} = 1.0 \times m_e = 9.109 \times 10^{-31}$ kg, and $T = 300$ K. For the discussion of electron transport and figure 3-6 we use $t_{\text{ox}} = 300$ nm, $L_c = 1000$ nm, $d_{\text{NW}} = 20$ nm, $\Phi_{\text{SB}} = 0.50$ eV, and $V_{\text{SD}}^{\text{max}} = 0.5$ V, unless stated differently. For the discussion of hole transport and figure 7-8 we use $t_{\text{ox}} = 300$ nm, $d_{\text{NW}} = 21$ nm, $\Phi_{\text{SB}} = 0.44$ eV, $V_{\text{SD}}^{\text{max}} = 2$ V. The 3D electrostatic potential $U_{ES}(x, y, z)$ for each combination of V_L , V_R , and V_G is calculated by solving Poisson equation with a commercial FEM software (COMSOL multiphysics.³⁶) The boundary potentials for the source, drain and gate contacts are kept constant at V_L , V_R , and V_G , respectively. The finite element mesh for the modeled structures is automatically generated with controlled distribution and increased density in the regions close to the insulator and NiSi₂/Si interfaces. The 1D potential profile $U_{ES}(x)$ along the axis of the NW is extracted from $U_{ES}(x, y, z)$.

IV. RESULT AND DISCUSSION

A. Dependence of the electrostatic potential on device geometries

As a first examination of the relationship between the geometry of FET devices and the efficiency of the gate effect, we have calculated 3D electrostatic potentials of FET devices. Figure 3(a) and (b) depict the potential landscapes with a gate potential of $V_G = 20$ V and the absence of a source-drain voltage. Figure 3(c) and (d) show the same potential along the axes of the channels for long and short silicon channels, respectively. In figure 3(a) and (c), the potential along the silicon channel drops strongly due to the applied gate field, whereas the gate field does not penetrate efficiently in the shorter silicon channel in figure 3(b) and (d).

In addition we have analyzed the influence of the thickness of the insulating layer between the nanowire device and the gate on the Schottky-barrier width. The Schottky-barrier width L_{SB} of the left interface is defined by the position $x = L_{\text{SB}} > 0$ satisfying

$$U(L_{\text{SB}}) = \mu_L. \quad (1)$$

In figure 4, we show the Schottky-barrier width of the FET devices as a function of applied gate voltage with varying thickness of the gate insulators and the chan-

nel lengths. We can see that the gate field reduces the Schottky-barrier width for all devices. We find that the Schottky-barrier width is inversely proportional to the gate voltage. The reduction of the silicon channel length as well as an increase of the width of the oxide layer prevents the gate field from efficiently penetrating into the Schottky-contact, leaving the Schottky-barrier width thicker than the device with long channel or an thick oxide layer. Since the gate voltage narrows the Schottky barrier the enhancement of the electron tunneling by the gate field is larger through SB-FET devices with longer silicon channels and thinner gate insulators.

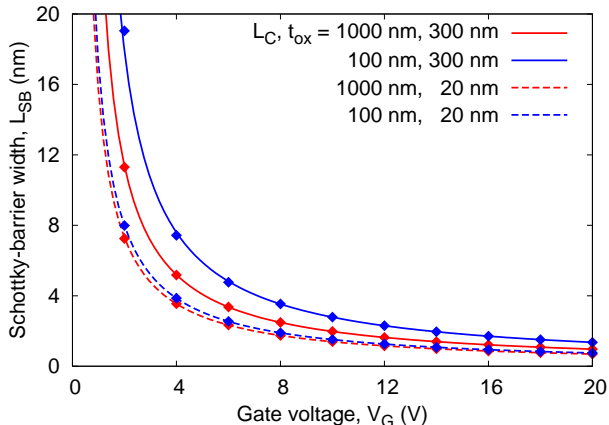


FIG. 4: Dependence of Schottky-barrier width L_{SB} on the gate voltage V_G , the channel length L_c , and the thickness of the oxide layer t_{ox} . L_{SB} is defined in figure 1. The continuous lines are fits of the data points to $L_{SB} = cV_G^{-1}$, i.e., the Schottky-barrier width is inversely proportional to the gate voltage. The gate effect is most efficient for large channel lengths and thin oxide layers.

B. Transmission function and I-V characteristics

Figure 5 shows potential profiles $U(x)$ at the left interface for different gate voltages and the corresponding transmission functions $T_L(E)$ for *electron* transmissions through these Schottky-barriers. The non-zero transmissions are due to the quantum tunneling effect. Since a positive gate voltage causes the Schottky-barrier to get thinner, the electron transmission increases with increasing gate voltage. For electrons with energies above the Schottky-barrier height Φ_{SB} , the electron transmission quickly approaches its maximum value 1. Therefore our model takes into account both tunneling currents and thermo-activated (thermionic) currents.

After calculating the transmission functions for both left and right interfaces, we have calculated the I-V characteristics of SB-FET devices by integrating over the total transmission function. Figure 6(a) shows the calculated drain current I_{SD} versus source-drain voltage V_{SD} for different gate voltages. The I-V curves show typical

features of conventional FETs, i.e., a linear increase of current followed by current saturation for higher source-drain voltages. The saturation currents are strongly enhanced with increasing gate fields leading to a typical switching behavior with a high on/off-current ratio. We evaluated this behavior by calculating the drain current at a fixed source-drain voltage for several gate voltages. Figure 6(b) presents the saturated drain current versus the gate voltage for a fixed source-drain voltage $V_{SD} = 0.5$ V. The drain current increases exponentially with the increase of the gate field in the lower gate voltages. This is due to the rapid reduction of the Schottky-barrier width with the increase of gate fields as shown in the figure 4. The saturation of the drain current in higher gate field can also be explained from the figure 4 since the Schottky-barrier width does not decrease so much in the higher gate field. The huge on/off-current ratio implies that the device is promising for logic operations. The flatness of the current in the saturation region in figure 6(a) is also beneficial for the logic operation since the current retains constant with respect to fluctuation of the source-drain voltage.

C. Comparison with experiment

Many measurements of SB-FETs consisting of SiNWs have exhibited unipolar p-type transfer characteristics,^{10–13,25} thus the current is transported by holes in these systems. As discussed previously, our model can also be applied to hole transport systems. In order to check the validity of the model, we have applied our model to SiNW-based SB-FETs and compared the I-V characteristics and on/off-current ratios with the experimental results measured by Weber *et al.*¹⁰

The numerical parameters are set as follows. The Schottky-barrier height between Ni-silicide and bulk Si ranges from 0.35 eV to 0.47 eV for holes.³⁷ Thus, we set the Schottky-barrier height of the NiSi₂/Si interface for holes as $\Phi_{SB} = 0.44$ eV. The diameter of the SiNWs is set to $d_{NW} = 21$ nm, identical to the mean diameter of the literature.¹⁰ The oxide thickness on the gate is set to $t_{ox} = 300$ nm.

Figure 7 presents the calculated drain currents I_{SD} versus source-drain voltage V_{SD} for (a) long ($L_c = 1000$ nm) and (b) short gate length ($L_c = 200$ nm) with experimental data provided by Weber *et al.*¹⁰ The calculated I-V curves for both systems exhibit similar features as the experimental results having both a linear increase and saturation at higher source-drain voltages. The drain current through the shorter channel is smaller than the one through the longer channel since the gate field does not optimally penetrate the NiSi₂/Si interfaces. Although the slopes of the calculated I-V curves for low source-drain voltages significantly exceed experimental ones, the amount of the saturated drain current shows a good agreement with the experiment except for the currents with high gate field.

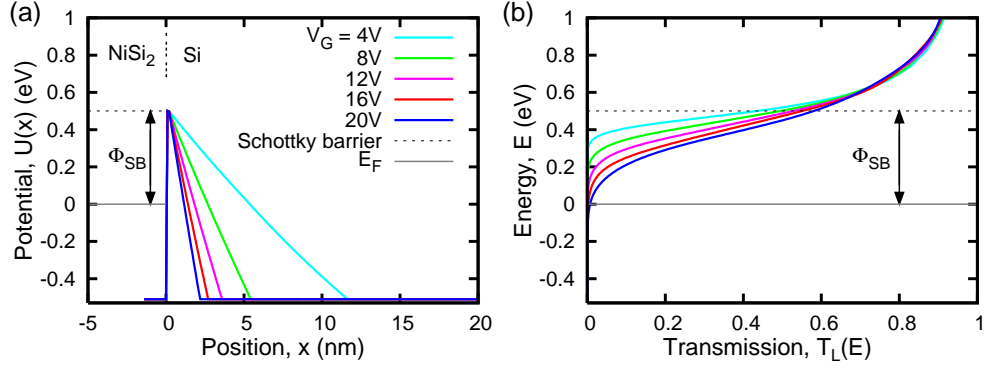


FIG. 5: (a) The potential profile $U(x)$ across the central axis of the left NiSi₂/Si interface for different gate voltages V_G , and (b) the corresponding transmission functions $T_L(E)$. Here the Schottky-barrier height $\Phi_{SB} = 0.50$ eV.

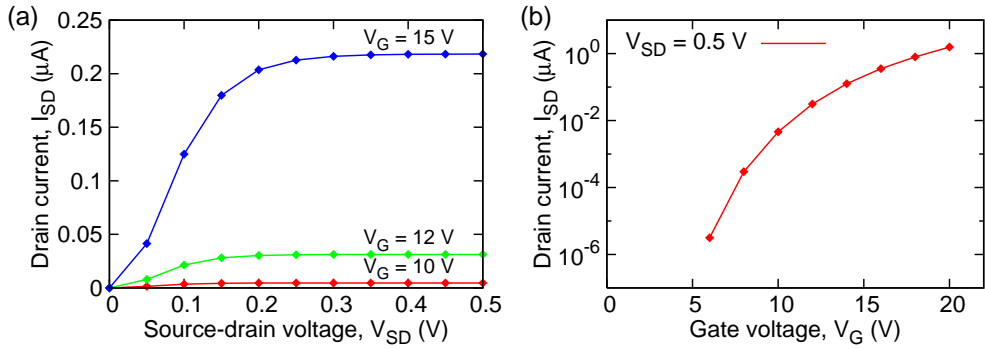


FIG. 6: Electron transport characteristics of the SB-FET device. (a) Drain current I_{SD} versus source-drain voltage V_{SD} for different gate voltages V_G . The drain current saturates at higher bias voltages. The saturated current is significantly enhanced with higher gate voltages. (b) Drain current I_{SD} versus gate voltage V_G for a fixed source-drain voltage ($V_{SD} = 0.5$ V). We obtain the typical behavior of a conventional FET device.

Figure 8 presents the saturated drain current versus the gate voltage of SB-FET devices with long and short channels. The saturated drain currents increase significantly with the increase of the gate field since the gate field reduces Schottky-barrier width as shown figure 4. The on-currents in the short and long systems are of the same order of magnitude. On the other hand, the off-currents for small gate voltages are significantly smaller for the short channel. Although the drain current in the lower gate field is underestimated, the numerical results show a qualitative agreement with experiment. Generally we observe that the drain currents of the SB-FET with the long channel are higher than for the short channel because the gate effect is more efficient (compare figure 3(c), (d), figure 4, and figure 7(a), (b)).

The discrepancies between our model and the experiment come from the simplicity of our model. First, we did not take into account the sub-bands^{27,38,39} but expressed the transport by using a single band model. The inclusion of the sub-bands will lower the drain current for small source-drain voltages since the onset of current flow through the channel will be shifted to higher

source-drain voltages due to the difference of energies between sub-bands. In addition, the reconstruction of the exact potential profile at the Schottky-contact^{40,41} due to space-charge effects and the dependence of the potential on the lateral position in the wire are not considered in this study. Furthermore, the effect of capacitance at the left and right interfaces and at the gate contact are not included.⁴² The addition of a native SiO₂ layer on the surface of the nanowire and the corresponding change of the electronic structures between the core and surface of the nanowire will also have an impact on the transport properties.⁴³ In order to capture the underlying physics of SB-FET devices, an advanced model incorporating these effects will be needed. Further studies including these effects will give helpful information for the future development of nanowire-based FET devices.

V. CONCLUSION

In summary, nanowire-based FETs have been focusing attention as a promising platform for sensor applica-

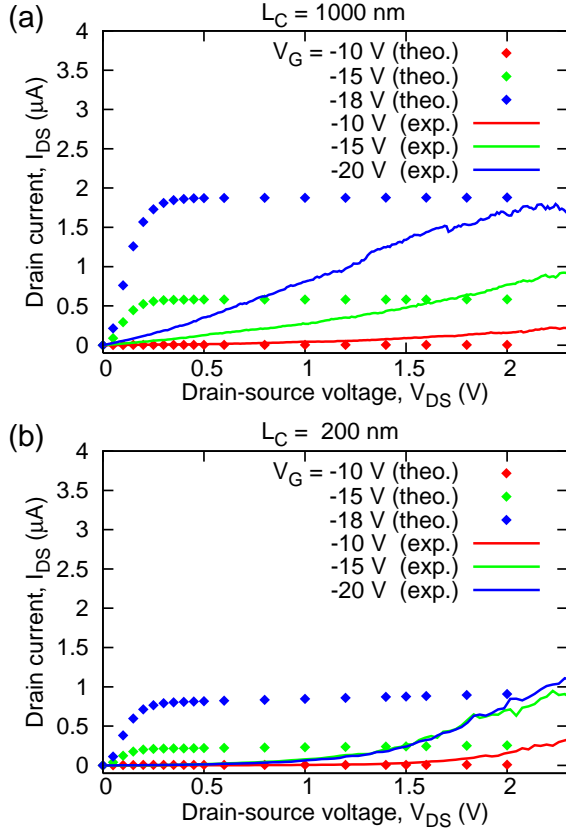


FIG. 7: I-V characteristics of two FET devices for (a) a long and (b) a short channel length at different gate voltages. The calculated currents are shown with dots. The experimental results given by Weber *et al.*¹⁰ are shown as continuous lines for comparison. Although the theoretical currents reach their saturations at lower bias, the saturated currents show a good agreement with experiments. Note that $I_{DS} = -I_{SD}$ and $V_{DS} = -V_{SD}$.

tions due to their high sensitivity. In order to understand the origin of the physical behavior in the nanowire-based FET devices, we have developed a multiscale model combining classical FEM and the Landauer approach. Our model is conceptually simple, computationally inexpensive, it uses only a few empirical parameters, and it is possible to simulate devices with dimensions ranging from a few nanometers up to some micrometers. We have applied this model to Schottky-barrier FETs consisting of SiNWs working as channel and NiSi₂ NW working as source and drain contacts. Our calculated I-V characteristics showed the typical behavior of conventional FET devices, having a linear increase of current followed by a saturation. The saturated drain currents increase with increasing gate field due to the reduction of the Schottky-barrier width. Despite the simplicity of the model, the calculations showed a good agreement with experiments and the model correctly reproduces the dependence of the saturated drain current on the gate field and the device geometry.

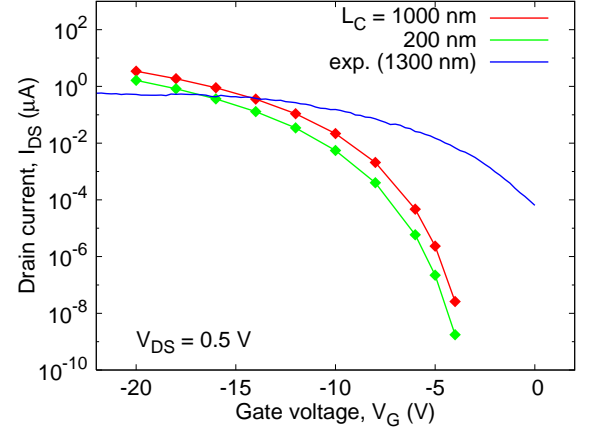


FIG. 8: Drain current I_{DS} versus gate voltage V_G characteristics of SiNW-based SB-FET devices with long (in red) and short (in green) silicon channels. The source-drain voltage is fixed to be $V_{DS} = 0.5$ V. For comparison, the experimental results of Weber *et al.*¹⁰ for a long (1300 nm) SiNW are shown (in blue). Numerical results show a qualitative agreement with experiment. The drain currents of the SB-FET with the long channel are higher than for the short channel because the gate effect is more efficient.

Our approach is suitable for one-dimensional Schottky-barrier field-effect transistors of arbitrary device geometry. The model can be improved by taking into account for example insulating layers surrounding the nanowires, the deformation of the electrostatic potential at the Schottky-contacts, or accurate electronic band dispersions. The results obtained from our model will serve as guidelines for the understanding of ongoing experimental work and will help in the design of device architectures for future applications.

Acknowledgments

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